CHIPSET SUPPORTING MULTIPLE CPU'S AND LAYOUT METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 90120461, filed August 21, 2001.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates in general to a control chipset of a computer motherboard, and more particularly, to a control chipset that supports various kinds of central processing units (CPU's) and a layout method thereof.

Description of the Related Art

[0002] As the personal computer rapidly develops, various kinds of CPU's are being manufactured. To comply with the variety of CPU's, motherboards able to support various kinds of CPU's are being developed. Further, because the processing speed of the CPU's continuously increases, signal transmission and reliability are of great concern to computer manufacturers. A good transmission quality results in better system performance and enhances reliability. Thus, how to fabricate a chipset with good signal transmission quality and reliability that supports various kinds of CPU's has become an important topic.

[0003] FIG. 1A and FIG. 1B are block diagrams showing a computer system accommodating a first type CPU and a second type CPU, respectively. Referring to FIGS. 1A and 1B, the chipset 110 (normally a north bridge chip, N/B) of a computer system can be coupled to a first type CPU 120 or a second type CPU 130, e.g., CPU 120 and 130 may be Intel PIII processor and AMD K7 processor, respectively.

[0004] Since Intel PIII processors require only one clock signal to perform data transactions with the N/B, while AMD K7 processor requires one input clock signal and one output clock signal to perform data transactions with the N/B, the output clock signal function is similar to the strobe signal. In the prior art, the N/B applied to the Intel PIII processor does not require an additional clock signal pin, while the conventional AMD K7 processor requires more than ten clock signal pins for the N/B. Thus, when designing a N/B applicable to both Intel PIII and AMD K7 processors, under the consideration of reserving I/O pin counts, the clock signal lines should share pins with other signal lines (such as the address (A/D) lines) via multiplexing mechanism.

[0005] FIG. 2 shows a conventional chipset that supports various CPU's. In FIG. 2, the chipset 210 is a north bridge including a first system logic circuit 220, a second system logic circuit 230, a first switch circuit 240, a second switch circuit 250, a first double defined signal pin 241, and a second double defined signal pin 251. The first system logic circuit 220 is applicable for the chipset coupled to an Intel PIII processor, while the second system logic 230 is applicable for the chipset coupled to the AMD K7 processor. When the chipset 210 is used for the AMD K7 processor, the first and second switch circuits 240 and 250 are used to control the connection switching

between the first and the second double defined signal pins 241, 251 with the second system logic circuit 230. Meanwhile, the second double defined signal pin 251 is connected to the clock signal CLK of the second system logic circuit 230 via the second switch circuit 250.

[0006] FIG. 3 shows the second switch circuit 250 composed of transmission gates. Referring to FIG. 3, the second switch circuit 250 includes a first transmission gate 310 and the second transmission gate 320. The first transmission gate 310 has a first terminal connected to an address signal line (HA_4 line), while the second transmission gate 320 has a first terminal connected to the clock signal line (CLK line). The second terminals of the first and the second transmission gates 310 and 320 are connected together for output. A control signal CTLA which indicates whether an Intel or AMD processor is coupled to the chipset 210 is used to control outputs of the second switch circuit 250. For example, HA_4 line is selected when the control terminal CTLA is high, and the CLK line is selected when the control terminal CTLA is low.

[0007] The above circuit and layout design has some drawbacks. Basically, signals with the same character can share one pin for signal transmissions. The above switch circuits controlling the transmissions at the signal pins are used for the Intel PIII processor or the AMD K7 processor. However, if signals with different characters such as HA_4 (address) and CLK (clock) in the second switch circuit 250 are multiplexed from a shared pin, e.g., the second double defined signal pin 251, unwanted crosstalk interference will be arisen during the signal transmission. As a result, the signal transmission quality is degraded. A conventional transmission gate is known as a non-ideal switch circuit for the north bridge chip. In high frequency applications, if a non-

linear circuit device (such as a transmission gate or TTL) is used as the transmission path for switching signals, the capacitance-induction effect may introduce unexpected ground bounce noises, which significantly degrades signal quality.

[0008] The clock signal and strobe signal are very high frequency signals in comparison with others. Therefore, when applying the conventional design to the chipset supporting more than one CPU, crosstalk interference will be arisen when multiplexing a pin shared by several signal lines especially that every one of the signal lines is usually too close to its adjacent ones. Further, undesired ground bounce noises will also be introduced when the multiplex switch circuit is configured by using transmission gates, which seriously affecting the signal transmission quality

SUMMARY OF THE INVENTION

[0009] The invention provides a chipset that supports multiple CPU's. The chipset includes a first system logic circuit connected to a first type CPU, a second logic circuit connected to a second type CPU, a double defined signal pin, an independent clock pin and a multiplex switch circuit. The independent clock pin coupled to the second system logic circuit is defined as the clock signal pin, which is not further defined as another signal pin. The multiplex switch circuit is coupled to the first system logic circuit, the second system logic circuit and the double defined signal pin so that the first signal from the first system logic circuit or the second signal from the second system logic circuit can be transferred via the double defined signal pin. The trace length connected between the independent clock signal pin and the second system logic circuit is shorter than before, and the spaces between the clock signal line and others are larger than that between two of the other adjacent signal lines.

[0010] The invention further provides a layout method of the chipset supporting multiple CPU's. The chipset comprises at least a first system logic circuit connected to a first type CPU and a second system logic circuit connected to a second type CPU. A double defined signal pin is provided for signal transmission under controlled by multiplexing mechanism. A multiplex switch circuit is provided and connected to the first system logic circuit, the second system logic circuit and the double defined signal pin. Thereby, the first signal of the first system logic circuit or the second signal of the second system logic circuit is connected to the double defined signal pin. An independent clock pin is provided for only one kind of signal. The second system logic circuit connects to the independent clock pin with a trace length shorter than that connected between other signal pins. The spaces between the clock signal line and other signal lines are larger than before, and furthermore, are also larger than the spaces between other signal lines, such as the spaces between two adjacent lines of the address or control signal lines.

[0011] The invention provides a chipset to support various kinds of CPU's and a layout method thereof. A signal such as the clock signal that usually operates under high frequency uses an independent pin without being multiplexed with other signal lines, which significantly eliminates the disadvantage of interference caused from line-sharing with others . The signal transmission quality is thus enhanced. In the embodiment, the clock signal is isolated from other signals, which indicates that the length for the second system logic circuit connecting with the independent clock pin is shorter than before. Furthermore, the connection length is also shorter than that with other signal lines, e.g., address lines or control signal lines. The spaces between the independent clock line with others are also larger than before in the embodiment.

Several advantages are offered by the present invention. Firstly, all signals transferred in the embodiment can be prevented from over attenuation. And secondly, the complexity of chipset circuits are simplified so that an efficient way is suggested for layout designs.

[0012] Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIGS. 1A and 1B shows a block diagram of a chipset that can support a first type CPU and a second type CPU;

[0014] FIG. 2 a conventional chipset that can support multiple CPU's;

[0015] FIG. 3 shows a switch circuit formed of transmission gates; and

[0016] FIG. 4 shows an embodiment of a chipset that supports various kinds of CPU's.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] Referring to FIGS. 1A and 1B, the chipset for supporting various kinds of CPU's can be applied to computer systems or the likes. To achieve the objective of supporting two different kinds of CPU's, the chipset provided by the invention can be coupled to a first type CPU or a second type CPU. The first type CPU includes the Pentium series of CPU such as the PIII processor, and the second type CPU includes the

AMD series CPU such as the AMD K7 processor.

[0018] The Intel PIII processor requires only one kind of clock signal to perform data transaction and transmission with a north bridge chip. On the other hand, the AMD K7 processor requires an input clock signal and an output clock signal that the output clock signal is functioned similarly as a strobe signal to transact and transmit data with the north bridge. While designing a north bridge chip to support these two CPU's, it is realized that less clock signal pins are needed for the Intel processors than that for the AMD K7 processor. In the embodiment, any high frequency signal with different characteristics from other signals will be delivered by an independent signal pin. For example, the clock signal for the AMD K7 signal is transferred by an independent signal pin that is isolated from the other signal pins for the Intel PIII processor.

[0019] From the view point of the motherboard designer, the chipset has a plurality of pins including the independent clock pin and a plurality of double defined signal pins. The independent clock pin is coupled to the second type of CPU as a clock signal pinthat is not connected to the first type CPU. Other double defined signal pins can be coupled to the first type CPU or the second type CPU by means of switch circuits. When the chipset couples to the first type CPU, the double defined signal pins are defined as the signal pins for the first type CPU. When the chipset couples to the second type CPU, the double defined signal pins are defined as the signal pins for the second type CPU.

[0020] FIG. 4 shows the chipset supporting multiple CPU's of the invention. Referring to FIG. 4, the chipset 410 supporting multiple CPU's comprises at least a first

system logic circuit 420, a second system logic circuit 430, a double defined signal pin 441, an independent clock pin 431 and a multiplex switch circuit 440. The so-called system logic circuit means the internal logic control circuit in a typical chipset. The first system logic circuit is applicable to the chipset 410 and is connected to the first type CPU. The second system logic circuit is applicable to the chipset 410 and is connected to the second type CPU. The first type CPU includes a Pentium series CPU such as PIII processor, and the second type CPU includes an AMD series CPU such as AMD K7 processor.

[0021] The multiplex switch circuit 440 of the chipset 410 is coupled to the first system logic circuit 420, the second system logic circuit 430 and the double defined signal pin 441. The signals of the first system logic circuit 420 and the second system logic circuit 430 are thus connected to the double defined signal pin 441. That is, when the chipset 410 couples to the Intel PIII processor, the chipset 410 controls the multiplex switch circuit 440 to establish a first connection between the double defined signal pin 441 and the first system logic circuit 420. Similarly, when the chipset 410 has to couple with the AMD K7 processor, a second connection between the double defined signal pin 441 and the second system logic circuit 430 is also established via the multiplex switch circuit 440. An Intel or AMD processors may transfer signals via the first or second connections, respectively. A control signal CTLA (not shown in FIG. 4) described in the background may be used to control outputs of the multiple switch circuit 440 so that associated connections can be established according to employed processors.**[0022]** The invention is characterized by coupling the independent clock pin 431 to the second system logic circuit 430 as the clock signal pin, and the independent clock pin 431 is isolated from other signals. That is, when the chipset 410 is coupled to

the AMD K7 processor, the connection between the second system logic circuit 430 and the AMD K7 processor via an independent clock pin forms an isolation path without coming across any multiplex circuit. The clock signal line connected between the independent clock pin and the second system logic circuit is shorter than that between other signal lines. For example, the trace length (connection length) of the independent clock pin is significantly shorter than before because the independent clock pin directly connects with associated clock signal pins without coming across any switch circuit (e.g., the second switch circuit 250). Therefore, every trace length of address line or control signal line in chipset 410 should be longer than that of the independent clock pin. Further, the spaces between the independent clock pin and the other signal lines are larger than that between two adjacent lines of the other signal lines. For example, each address or control signal line may be closer to its adjacent ones, which significantly decreases the spaces between two adjacent ones of the address or control signal lines, however, the independent clock pin does not follow this constraint. The circuit complexity of chipset 410 is simplified and an efficient way is suggested for layout designs.

[0023] It is appreciated to people having ordinary skills in the art that the above clock signals such as the strobe signal or other clock signals are high frequency signals with different signal quality. If the second type CPU has such strobe signals, clock signals, or the likes, the chipset 410 should allocate independent signal pins 432 for delivering signals for them.

[0024] Accordingly, a layout method for a chipset that supports multiple CPU's is provided by the invention. The chipset comprises a first system logic circuit and a

second system logic circuit. A least one double defined signal pin is provided firstly that every double defined signal pins is used as signal transmission pins. A multiplex switch circuit is provided and connected to the first system logic circuit, the second system logic circuit and the double defined signal pins. The multiplex switch circuit can be connected to either the first system logic circuit or the second system logic circuit according to an indication of a control signal (e.g., CTLA). An independent clock pin is provided for delivering only one kind of signal. The independent clock pin is connected to the clock signal of the second system logic circuit with a signal line shorter than that between other signal pins. Further, the spaces between the clock signal line and other signal lines are larger than that between other signal lines.

[0025] The chipset and layout method of the invention separate and isolate the high frequency signals such as the clock or strobe signals, so that every pin for delivering such high frequency signals is isolated and multiplexed with other signal lines. Advantages as follows are thus obtained:

1. The fatal noise interference during signal transmission is reduced.

2. The internal circuit complexity of the chipset is reduced.

3. The trace layout for the chipset is easy to make.

[0026] Other embodiments of the invention will appear to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples are to be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.